2416

16,384 BIT CCD SERIAL MEMORY

▪ Organization: 64 Recirculating Shift Registers of 256 Bits Each

- **Avg. Latency Time Under 100 μs**
- **Max. Serial Data Transfer Rate —2 mega bits/sec.**
- **Address Registers Incorporated on Chip**
- **Standard Power Supplies— +12V, −5V**
- **Open Drain Output**
- **Combined Read/Write Cycles Allowed**
- **Compatible to Intel® 5244 CCD Driver**

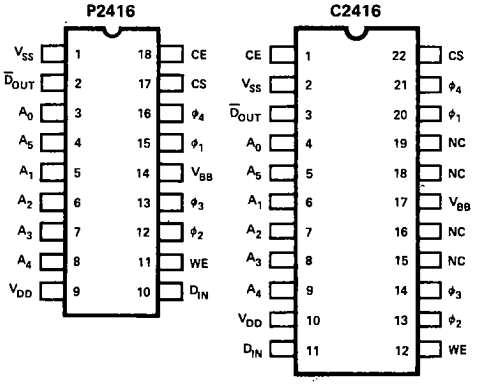
The Intel®2416 is a 16,384 bit CCD serial memory designed for low-cost memory applications requiring average latency times to under 100 μs. To achieve low latency time the memory was organized in the form of 64 independent recirculating shift registers of 256 bits each. Any one of the 64 shift registers can be accessed by applying an appropriate 6-bit address input.

The shift registers recirculate data automatically as long as the four-phase CCD clocks (ϕ_1 . . . ϕ_4) are continuously applied and no write command is given. A one-bit shift is initiated in all 64 registers following a low-to-high transition of either ϕ_2 or ϕ_4. After the shift operation the contents of the 64 registers at the bit location involved are available for non-destructive reading, and/or for modification. I/O functions are accomplished in a manner similar to that of a 64-bit dynamic RAM. At the next shift cycle, the contents of the 64 accessible bits (whether modified or not) are transferred forward into the respective registers and the contents of the next bit of each register become accessible. No I/O function can be performed during the shift operation itself.

The Intel 2416 generates and uses an internal reference voltage which requires some time to stabilize after the power supplies and four phase clocks have been turned on. No I/O functions should be performed until the four-phase CCD clocks have executed at least 4000 shift cycles with power supplies at operating voltages. After this start-up period, no special action is needed to keep the internal reference voltage stable.

The 2416 is fabricated using Intel's advanced high voltage N-channel Silicon Gate MOS process.

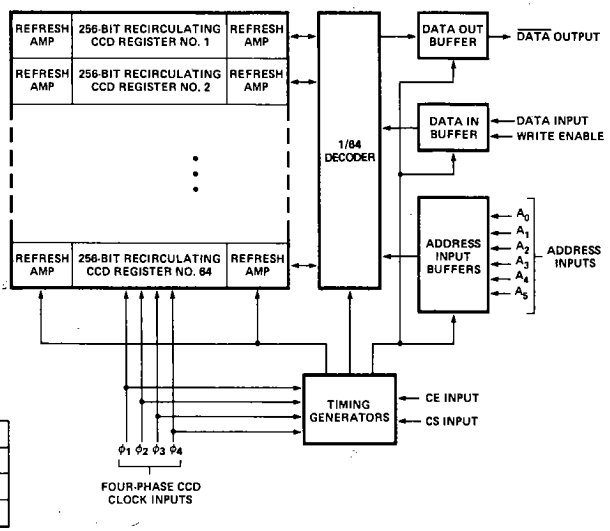
PIN CONFIGURATIONS



PIN NAMES

A_0-A_5	ADDRESS INPUTS	CE	CHIP ENABLE INPUT
D_{IN}	DATA INPUT	ϕ_1-ϕ_4	CCD CLOCK INPUTS
WE	WRITE ENABLE INPUT	V_{DD}, V_{SS}, V_{BB}	POWER SUPPLIES
CS	CHIP SELECT INPUT	$\overline{D}_{OUT}$	DATA OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} . . . . . +25V to -0.3V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} . . . . . +20V to -0.3V
Power Dissipation 1.0W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{BB}[1] = -5V ±5%, V_{SS} = 0V, unless otherwise specified.

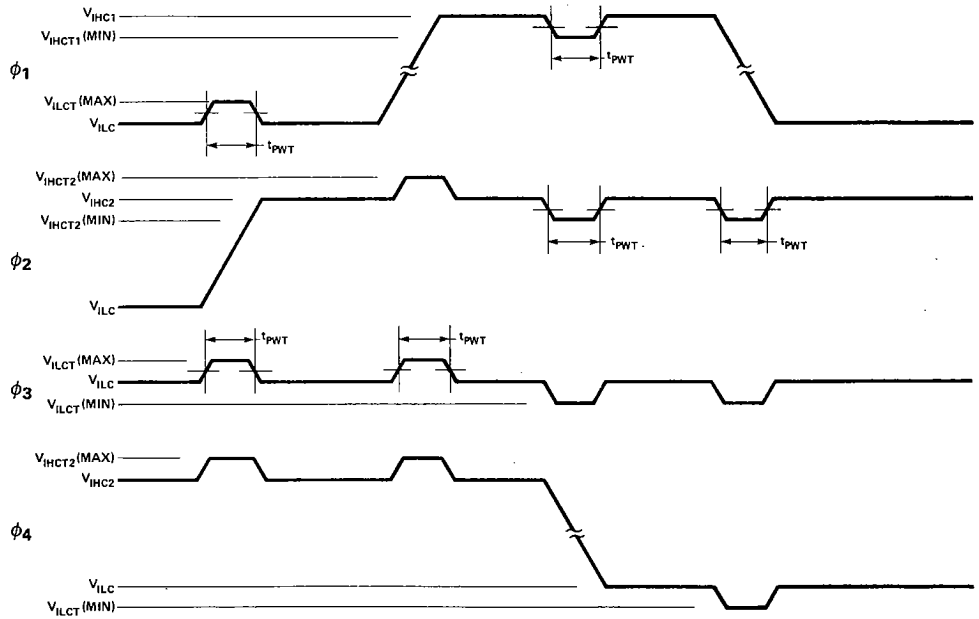
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_{LI}	Input Leakage Current		1	10	µA	V_{IN} = 0V
I_{LO}	Output Leakage Current		1	10	µA	CE = 0V, V_{OUT} = 0V
I_{OL}	Output Low Current	3			mA	V_{OL} = .45V
I_{OH}	Output High Current			10	µA	V_{OH} = +5V
I_{DDAV1}	Average V_{DD} Supply Current for Shift Cycles Only			Note 2	mA	
I_{DDAV2}[3]	Average V_{DD} Supply Current		15	25	mA	
I_{BB}	Average V_{BB} Supply Current		100	200	µA	
V_{IL}	Input Low Voltage, All Inputs Except $\phi_1 \ldots \phi_4$	-1.0		0.8	V	
V_{IH1}	Input High Voltage, All Inputs Except D_{IN} and $\phi_1 \ldots \phi_4$	V_{DD}-1		V_{DD}+1	V	
V_{IHD}	D_{IN} Input High Voltage	3.5		V_{DD}+1	V	
V_{ILC}[4]	$\phi_1 \ldots \phi_4$ Input Low Voltage dc	-2.0		0.6	V	
V_{ILCT}	$\phi_1 \ldots \phi_4$ Input Low Voltage w/Coupling	-2.0[5]		1.2[6]	V	
V_{IHC1}	ϕ_1 and ϕ_3 Input High Voltage dc	V_{DD}-1		V_{DD}+2	V	
V_{IHCT1}	ϕ_1 and ϕ_3 Input High Voltage w/Coupling	V_{DD}-1.6[6]		V_{DD}+2[5]	V	
V_{IHC2}	ϕ_2 and ϕ_4 Input High Voltage dc	V_{DD}-0.6		V_{DD}+2	V	
V_{IHCT2}	ϕ_2 and ϕ_4 Input High Voltage w/Coupling	V_{DD}-1.2[6]		V_{DD}+2[5]	V	
t_{PWT}	Cross Coupling Voltage Pulse Width			Note 7	ns	Pulse width measured at 0.8V and V_{DD}-1.2V (ϕ_1 and ϕ_3) or V_{DD}-0.8V (ϕ_2 and ϕ_4)

Notes: 1. The only requirement for the sequence of applying voltage to the device is that V_{DD} and V_{SS} should never be 0.3V more negative than V_{BB}.

2. For shift only mode $I_{DD} = 2.0mA + \frac{15mA}{t_{\phi/2}\ (\text{in } \mu s)}$

3. I_{DDAV2} is for combined shift and data I/O cycles.
4. The difference in the low level reference voltages between all four clock phases must not exceed 0.5 volts.
5. These voltage levels with coupling are within the specified dc range and are not, therefore, subject to t_{PWT} restrictions.
6. These voltage levels with coupling are outside specified dc ranges and must be restricted to t_{PWT} pulse widths.
7. The maximum clock cross coupled pulse width is the sum of the clock transition time (t_T) plus 20ns.

$\phi_1 \ldots \phi_4$ CROSS-COUPLING

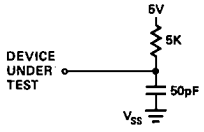


A.C. Characteristics T_A = 0°C to 70°C, V_{DD} = 12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, unless otherwise specified.

SHIFT ONLY CYCLES

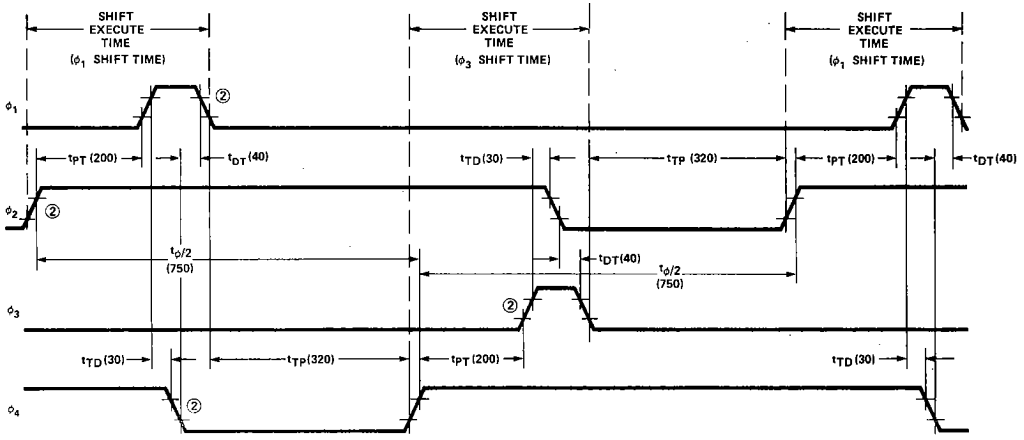
Symbol	Parameter	Min.	Max.	Unit	Conditions
$t_{\phi/2}$	Half Clock Period for $\phi_1 \ldots \phi_4$	750[1]	10,000	ns	t_T = 40nsec
t_{PT}	ϕ_2 On to ϕ_1 On Time, ϕ_4 On to ϕ_3 On Time	200		ns	
t_{TD}	ϕ_1 to ϕ_4 Overlap, ϕ_3 to ϕ_2 Overlap	30		ns	
t_{DT}	ϕ_4 to ϕ_1 Hold Time, ϕ_2 to ϕ_3 Hold Time	40		ns	
t_{TP}	ϕ_1 Off to ϕ_4 On, ϕ_3 Off to ϕ_2 On	320		ns	
t_T	Transition Times for $\phi_1 \ldots \phi_4$	30	200	ns	

$\bar{D}_{OUT}$ TEST LOAD



Note: 1. The 750ns Half Clock Period will be met for 30ns ≤ t_T ≤ 40ns. Values of t_T > 40ns lengthen $t_{\phi/2}$.

WAVEFORMS (Numbers in parentheses are for minimum cycle timing in ns)



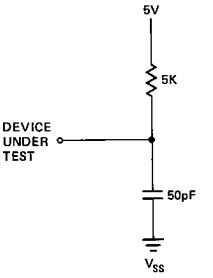
Note: 2. +2.0V and V_{DD}-2.0V are the reference low and high level respectively for measuring the timing of ϕ_1, ϕ_2, ϕ_3 and ϕ_4.

A.C. Characteristics

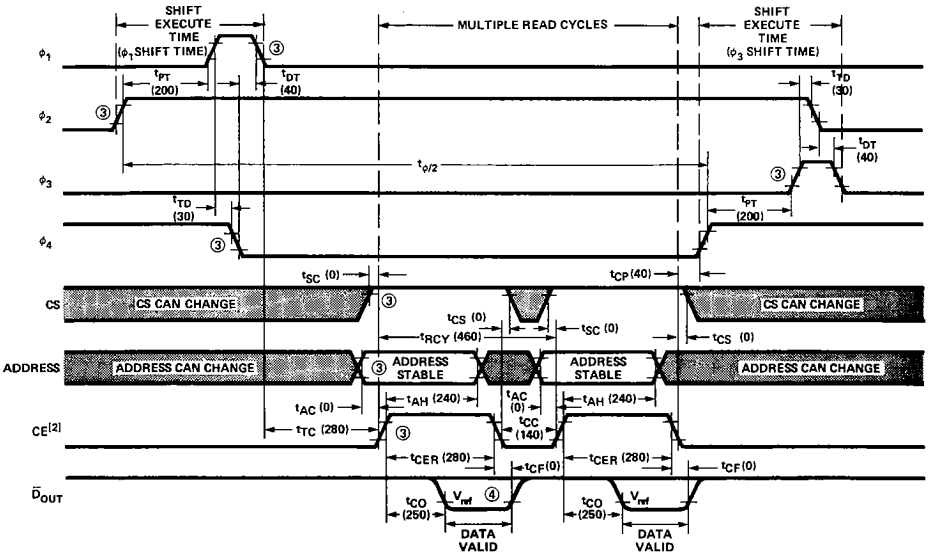
SHIFT–READ–READ–...–READ–SHIFT CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}	READ Cycle Time	460		ns	
t_{PT}	ϕ_2 On to ϕ_1 On Time, ϕ_4 On to ϕ_3 On Time	200		ns	t_T = 40ns
t_{TD}	ϕ_1 to ϕ_4 Overlap, ϕ_3 to ϕ_2 Overlap	30		ns	t_{T1} = 20ns
t_{DT}	ϕ_4 to ϕ_1 Hold Time, ϕ_2 to ϕ_3 Hold Time	40		ns	
$t_{\phi/2}$	Half Clock Period for $\phi_1 \ldots \phi_4$		10,000	ns	
t_T	Transition Times for $\phi_1 \ldots \phi_4$	30	200	ns	
t_{T1}	Transition Times for Inputs Other Than $\phi_1 \ldots \phi_4$		100	ns	
t_{TC}	ϕ_1 or ϕ_3 Off to CE On	280		ns	
t_{SC}	CS to CE Set-Up Time	0		ns	
t_{AC}	Address to CD Set-Up Time	0		ns	
t_{AH}	Address Hold Time	240		ns	
t_{CS}	CE to CS Hold Time	0		ns	
t_{CC}	CE Off Time	140		ns	
t_{CP}	CE Off to ϕ_2 or ϕ_4 On	40		ns	
t_{CER}	CE On Time	280		ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	
t_{CO}	CE to $\overline{D}_{OUT}$ Valid	250		ns	

$\overline{D}_{OUT}$ TEST LOAD



WAVEFORMS[1] (Numbers in parentheses are for minimum cycle timing in ns)



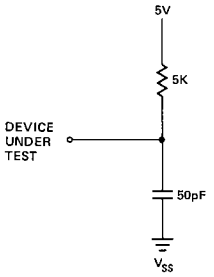
NOTES:
1. WE must be continuously low during the READ cycle.
2. When CE is off, the 2416 output level is determined by the external output termination.
3. +2.0V and V_{DD}-2.0V are the reference low and high level respectively for measuring the timing of $\phi_1 \ldots \phi_4$, CE, CS and addresses.
4. +0.8V is the reference level for measuring the timing of $\overline{D}_{OUT}$.

A.C. Characteristics

SHIFT–WRITE–WRITE–...–WRITE–SHIFT CYCLE

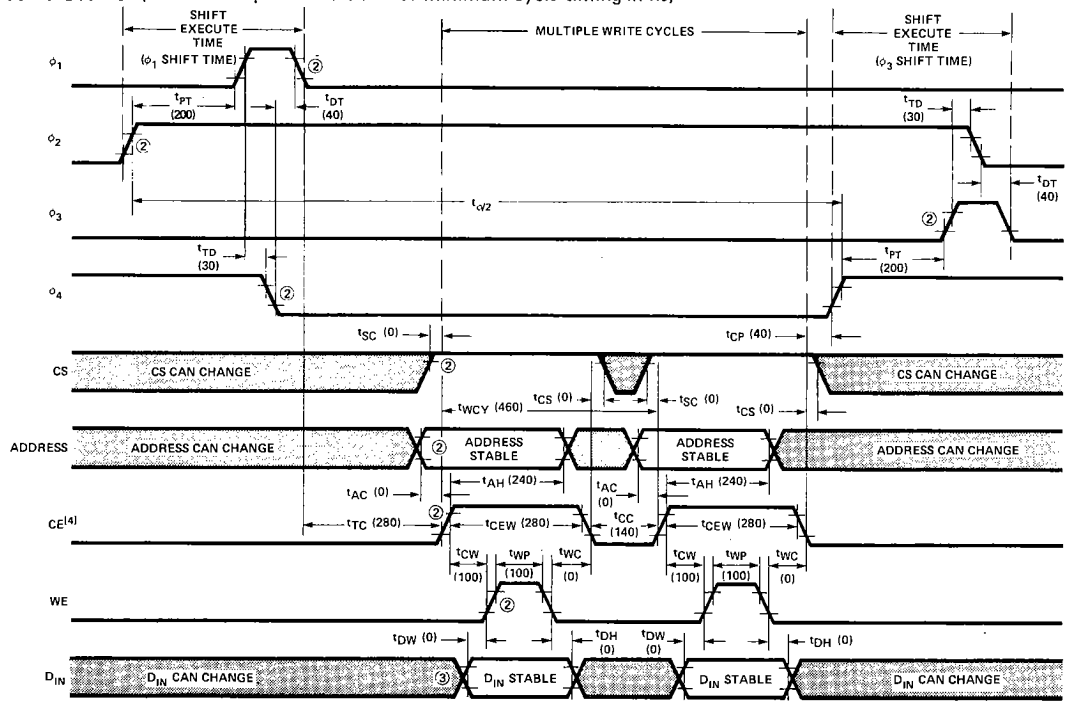
Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}	WRITE Cycle Time	460		ns	
t_{PT}	ϕ_2 On to ϕ_1 On Time, ϕ_4 On to ϕ_3 On Time	200		ns	t_T = 40ns
t_{TD}	ϕ_1 to ϕ_4 Overlap, ϕ_3 to ϕ_2 Overlap	30		ns	t_{T1} = 20ns
t_{DT}	ϕ_4 to ϕ_1 Hold Time, ϕ_2 to ϕ_3 Hold Time	40		ns	
$t_{\phi/2}$	Half Clock Period for $\phi_1 \ldots \phi_4$		10,000	ns	
t_T	Transition Times for $\phi_1 \ldots \phi_4$	30	200	ns	
t_{T1}	Transition Times for Inputs Other Than $\phi_1 \ldots \phi_4$		100	ns	
t_{TC}	ϕ_1 or ϕ_3 Off to CE On	280		ns	
t_{SC}	CS to CE Set-Up Time	0		ns	
t_{AC}	Address to CE Set-Up Time	0		ns	
t_{AH}	Address Hold Time	240		ns	
t_{CS}	CE to CS Hold Time	0		ns	
t_{CC}	CE Off Time	140		ns	
t_{CP}	CE Off to ϕ_2 or ϕ_4 On	40		ns	
t_{CEW}	CE On Time	280[1]		ns	
t_{CW}	CE to WE Set-Up Time	100[1]		ns	
t_{DW}	D_{IN} to WE Set-Up	0		ns	
t_{WP}	WE Pulse Width	100[1]		ns	
t_{WC}	WE Off to CE Off	0[1]		ns	
t_{DH}	D_{IN} Hold Time	0		ns	

$\overline{D}_{OUT}$ TEST LOAD



Note: 1. The minimum t_{CW}, t_{WP} and t_{WC} times with appropriate transitions do not necessarily add up to the minimum t_{CEW}. This allows the user flexibility in setting the WE Pulse Width edges without affecting either t_{CEW} or the WRITE Cycle Time, t_{WCY}.

WAVEFORMS (Numbers in parentheses are for minimum cycle timing in ns)

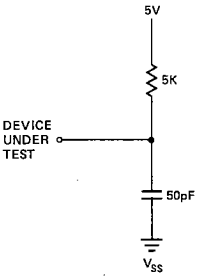


Notes: 2. +2.0V and V_{DD}–2.0V are the reference low and high level respectively for measuring the timing of $\phi_1 \ldots \phi_4$, CE, CS, WE, and addresses.
3. +1.5V and +3.0V are the reference low and high level respectively for measuring the timing of D_{IN}.

A.C. Characteristics SHIFT–RMW–RMW– . . . –RMW–SHIFT CYCLE

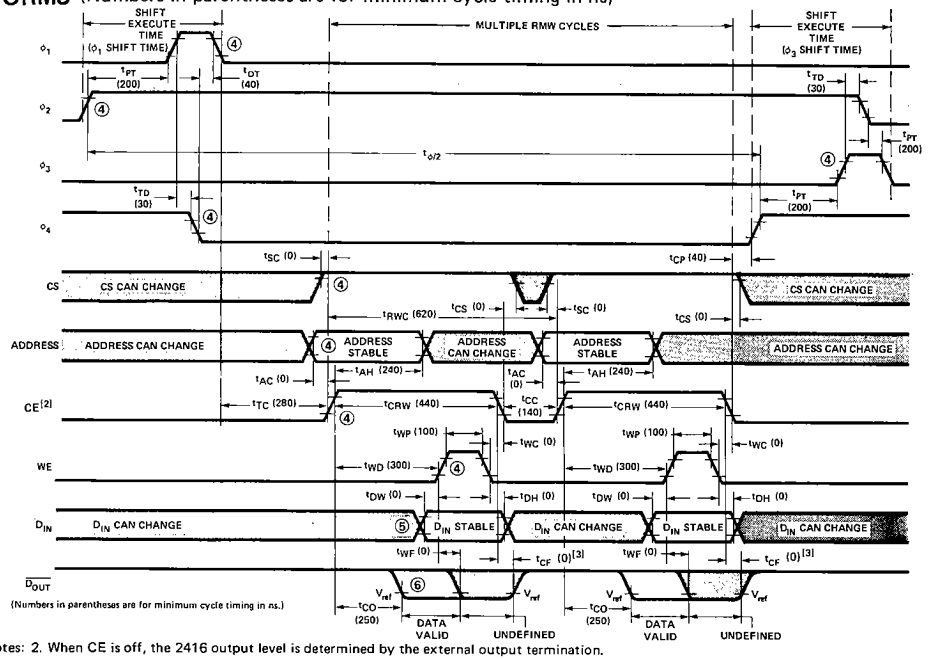
Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}	READ-MODIFY-WRITE Cycle Time	620		ns	
t_{PT}	ϕ_2 On to ϕ_1 On Time, ϕ_4 On to ϕ_3 On Time	200		ns	t_T = 40ns
t_{TD}	ϕ_1 to ϕ_4 Overlap, ϕ_3 to ϕ_2 Overlap	30		ns	t_{T1} = 20ns
t_{DT}	ϕ_4 to ϕ_1 Hold Time, ϕ_2 to ϕ_3 Hold Time	40		ns	
$t_{\phi/2}$	Half Clock Period for $\phi_1 \ldots \phi_4$		10,000	ns	
t_T	Transition Times for $\phi_1 \ldots \phi_4$	30	200	ns	
t_{T1}	Transition Times for Inputs Other Than $\phi_1 \ldots \phi_4$		100	ns	
t_{TC}	ϕ_1 or ϕ_3 Off to CE On	280		ns	
t_{SC}	CS to CE Set-Up Time	0		ns	
t_{AC}	Address to CE Set-Up Time	0		ns	
t_{AH}	Address Hold Time	240		ns	
t_{CS}	CE to CS Hold Time	0		ns	
t_{CC}	CE Off Time	140		ns	
t_{CP}	CE Off to ϕ_2 or ϕ_4 On	40		ns	
t_{CRW}	CE On Time	440[1]		ns	
t_{CO}	CE On to $\overline{D}_{OUT}$ Valid	250		ns	
t_{DW}	D_{IN} to WE Set-Up Time	0		ns	
t_{WP}	WE Pulse Width	100[1]		ns	
t_{WC}	WE Off to CE Off	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WD}	CE On to WE On	300[1]		ns	
t_{WF}	WE to $\overline{D}_{OUT}$ Undefined	0		ns	

$\overline{D}_{OUT}$ TEST LOAD



Note: 1. The minimum t_{WD} and t_{WP} times with appropriate transitions do not necessarily add up to the minimum t_{CRW}. This allows the user flexibility in setting the WE Pulse Width edges without affecting either t_{CRW} or the READ-MODIFY-WRITE Cycle Time, t_{RWC}.

WAVEFORMS (Numbers in parentheses are for minimum cycle timing in ns)



Notes: 2. When CE is off, the 2416 output level is determined by the external output termination.
3. The parameter t_{CF} is the same as in the Shift-Read-Shift Cycle on page 4.
4. +2.0V and V_{DD}-2.0V are the reference low and high level respectively for measuring the timing of $\phi_1 \ldots \phi_4$, CE, CS, WE, and addresses.
5. +1.5V and +3.0V are the reference low and high level respectively for measuring the timing of D_{IN}.
6. +0.8V is the reference level for measuring the timing of $\overline{D}_{OUT}$.

A.C. Characteristics

CAPACITANCE[1] $T_A = 25°C$

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Address, D_{IN}, CS, CE, WE Capacitance	4	6	pF	$V_{IN} = V_{SS}$
C_{OUT}	$\overline{D}_{OUT}$ Capacitance	3	5	pF	$V_{OUT} = V_{SS}$
$C_{\phi1}$[1], $C_{\phi3}$[2]	ϕ_1, ϕ_3 Input Capacitance	350	500	pF	$V_\phi = V_{SS}$
$C_{\phi2}$[1], $C_{\phi4}$[2]	ϕ_2, ϕ_4 Input Capacitance	480	700	pF	$V_\phi = V_{SS}$
$C_{\phi1-\phi2}$	Clock ϕ_1 To Clock ϕ_2 Capacitance	120	175	pF	$V_\phi = V_{SS}$
$C_{\phi1-\phi4}$	Clock ϕ_1 To Clock ϕ_4 Capacitance	150	200	pF	$V_\phi = V_{SS}$
$C_{\phi3-\phi2}$	Clock ϕ_3 To Clock ϕ_2 Capacitance	150	200	pF	$V_\phi = V_{SS}$
$C_{\phi3-\phi4}$	Clock ϕ_3 To Clock ϕ_4 Capacitance	120	175	pF	$V_\phi = V_{SS}$

Notes: 1. This parameter is periodically sampled and is not 100% tested.
2. The $C_{\phi1}$ .... $C_{\phi4}$ input clock capacitance includes the clock to clock capacitance. The equivalent input capacitance is given below.

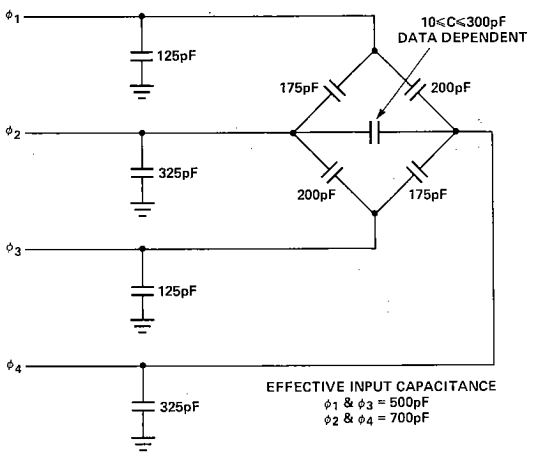
Four-Phase Clock Inputs

The four-phase clock inputs are internally connected to long electrodes used for several thin-oxide gates, resulting in high capacitance to the substrate on the clock inputs. In addition, considerable cross-coupling between adjacent clock exists due to the overlapping structure of the electrodes. The figure to the right shows the circuit equivalent of the clock inputs, indicating maximum capacitance values.

The equivalent circuit suggests two opposed clock driver requirements:

1. Ability to drive high-capacitance loads quickly.
2. Ability to suppress cross-coupled current transients.

The first requirement could ordinarily be met rather easily, if it weren't for the fact that the cross-coupled current, I, is proportional to the rate of change of the voltage, i.e., $I = C\frac{dv}{dt}$. For the quiescent driver to hold the coupled voltage to a minimum, the driver must have very low output impedance. However, when this driver becomes active the low output impedance increases the slope of the transitions which in turn increases coupling currents to the other drivers. This suggests that a driver have a controlled output transition time and a low output impedance characteristic in the quiescent state (high or low level). The Intel® 5244 meets these requirements.



5244 — CCD Clock Driver

The Intel® 5244 is a CMOS implemented fully TTL input compatible high voltage MOS driver, designed especially for the four phase clock inputs of the 2416. The device features very low DC power dissipation from a single +12V supply with output characteristics directly compatible with the 2416 clock input requirements.

The 5244 uses internal circuitry to control the cross-coupled voltage transients between the clock phases generated by the 2416. This internal circuitry limits the transition time to a specified range so that excessively fast transitions (<30ns) do not occur on the clock line. The entire operation is transparent to the user.

The 5244 is designed to drive four 2416s, but can drive fewer devices when loaded with additional capacitance to prevent a speedup in the transition times. Additional information on this and other aspects of the 5244 can be found on the 5244 data sheet.

Application Information

The Intel® 2416 is a charge coupled device (CCD) containing 16,384 bits of dynamic shift register storage available in a standard 18 pin plastic package. To minimize latency time (access time to any given bit in the device), the 2416 has been organized as 64 registers containing 256 bits each and, therefore, any bit can be accessed with a maximum of 255 shift operations. Since the minimum shift cycle requires 750 ns, the maximum latency time for the 2416 is less than 200μsec.

Access to the 64 recirculating registers is performed in a random access mode. A six bit address selects one of the 64 registers for read, write, or read/modify/write operations. These random access operations are performed between shift operations, and can be performed in any number or sequence as long as the basic shift frequency is maintained.

Because of substrate leakage currents the charge coupled storage mechanism is dynamic in nature. To satisfy the refresh requirements of the 2416, one shift operation must be performed every ten microseconds. A shift operation is completed on the falling edge of clock phase ϕ_1 or ϕ_3 and random access cycles may occur only between (1) the falling edge of ϕ_1 and the rising edge of ϕ_4 or (2) the falling edge of ϕ_3 and the rising edge of ϕ_2. This refresh requirement limits the number of random access cycles between successive shift operations to a maximum of 16.

Random access operations are performed in a manner which is very similar to any random access memory (RAM). All random access cycles are initiated with the rising edge and terminated with the falling edge of CE (Chip Enable). Read operations are performed when WE (Write Enable) remains low throughout a CE cycle. Data is strobed into the memory whenever WE is strobed high during a CE cycle as illustrated in the appropriate timing diagrams. CS (Chip Select) controls only the input and output circuits and is only effective when CE is high.

Typical Current Transients vs. Time

The oscilloscope photos in Figures 1 and 2 show typical I_{DD} current transients during shift and I/O cycles. The typical I_{BB} current during a shift cycle is shown in Figure 3.

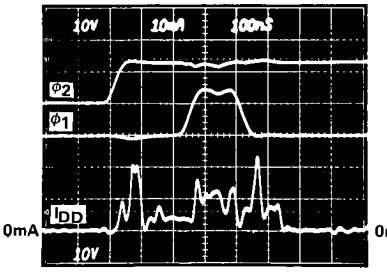


Figure 1. I_{DD} transient current during shift cycles.
I_{DD} scale: 10mA/div.

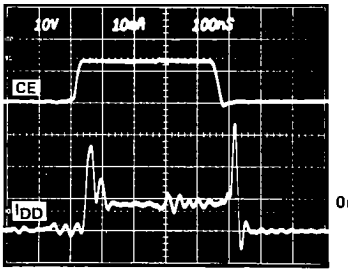


Figure 2. I_{DD} transient current during I/O cycles.
I_{DD} scale: 10mA/div.

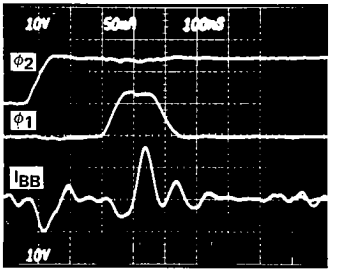


Figure 3. I_{BB} transient current during a shift cycle.
I_{BB} scale: 50mA/div.